Fakultät Wirtschaftsinformatik und Angewandte Informatik

Kolloquiumsvortrag
Donnerstag, 30.10. 2014, 16.15 Uhr, WE5/01.006

Network-on-Chip Design and Modelling for Low Power System-on-Chip

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This talk will focus at first on the process of building a System-on-Chip (SoC), from the idea all the way to the foundry. As SoCs have grown extremely complicated, so have the interconnects which bound the various components inside them. The second part of the talk will thus address the evolution of those interconnects and the necessary ingredients for a low power Network-on-Chip. An important part of the evolution of a NoC is given by the process of fast and accurate modelling.